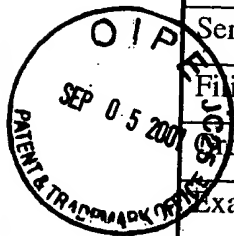


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Applicant(s)	Jack Linn et. al	<b>PRELIMINARY AMENDMENT</b>
Serial No.	Unknown	
Filing Date	Herewith	
Group Art Unit	Unknown	
Examiner Name	Unknown	
Attorney Docket No.	125.013US02	
Title: BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANER INTRINSIC GETTERING ZONE (as amended herewith)		

SEP 10 2001  
TC 2800 MAIL ROOM

Commissioner for Patents  
Box Patent Application  
Washington, D.C. 20231

Before taking up the above-identified patent application for examination, please amend it as follows.

09/14/2001 HARRIS 00000002 501373 09846795

01 FC:103 234.00 CH  
02 FC:162 160.00 CH

### IN THE TITLE

Please amend the title to read "BONDED SUBSTRATE FOR AN INTEGRATED CIRCUIT CONTAINING A PLANER INTRINSIC GETTERING ZONE".

### IN THE CLAIMS

Please amend claims 24, 26 and 30 and add new claims 38-56 as provided below:

24. (amended) A semiconductor device formed by the method comprising:  
providing a wafer comprising a monocrystalline semiconductor material;  
implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below

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